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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,586	08/19/2003	Nicolas I. Kacevas	02207/684502	2935

23838 7590 05/18/2005

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,586	KACEVAS, NICOLAS I.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-20* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1-14,17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani (patent No. 5,860,017) (submitted by applicant).

2. Sharangpani taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Bus (100) or bus coupled to cache and main memory (e.g., see fig. 1);

b) External memory (106,102,103,108);

c) Processor (101) coupled to the memory (102,103,106,108) via the bus (100 or the bus coupled to the cache and memory in fig. 1), the processor to receive a plurality of instructions from the memory, wherein the processor is to: advance an instruction in an instruction sequence predicted not to be executed through an instruction pipeline (e.g., see col. 3, line 41-col. 4, line 30).

3. Sharangpani did not expressly detail (claims 1,6,10,17) storing in a mispredicted path side memory in parallel a result of the instruction in the instruction sequence that is predicted not to be executed from the instruction pipeline, and restoring in parallel from the store into the instruction pipeline for continued execution if an instruction sequence predicted to be executed is mispredicted. Sharangpani however taught executing the predicted to be executed path of instructions and the predicted not to be executed path of instructions in parallel and when the branch was resolved using the path of the two paths that was correct according to the resolution of the branch and flushing the

incorrect path (e.g., see col. 7, lines 32-59 and col. 3, line 41-col. 4, line 30, and col. 11, lines 25-59). Since the storing of the results for each path would have been required in order not to lose the results one of ordinary skill would have been motivated to incorporate at least one memory for storing the results of both paths. Also since Sharangpani taught (claims 5,20) incorporation of a cache and main memory (and data cache 328, e.g., see col. 6, lines 20-27) which were well known in the art to store results from processing of instructions then one of ordinary skill would have been motivated to store results in the cache and/or main memory. Also since Sharanpani taught flushing the pipeline path that was incorrect one of ordinary skill would have been motivated to separately store the results from the each pipeline path so that the deleting of results from the incorrect path would be performed easily for efficiently executing the branch (e.g., see col. 7, lines 32-59 and col. 3, line 41-col. 4, line 46, and col. 11, lines 25-59) where the memory that stored the mispredicted path would have been the mispredicted path memory.

4. As per claims 2, 17, Sharangpani also taught the processor advanced the instruction in the instruction sequence predicted to be executed through the instruction pipeline (e.g., see col. 7, lines 32-59 and col. 3, line 41-col. 4, line 46).

5. As per claim 3,8,18 Sharangpani taught discarding of the instruction that was predicted not to be executed if the instruction in the sequence predicted to be executed was predicted correctly (e.g., see col. 3, line 41-col. 4, line 46).

6. As per claims 4,9,19 Sharangpani taught the processing of predicted to be executed path and predicted not to be executed path in the processing of a program when a branch instruction was encountered depending of the available resources and restoring the correct path and flushing the incorrect path. Therefore this procedure would have been performed for a first branch instruction when resources were available and performed for a second and subsequent branch instructions that would have been encountered depending on available resources (e.g., see col. 7, lines 32-59 and col. 3, line 41-col. 4, line 46, and col. 11, lines 25-59).

7. As to the predicting at the branch (claims 6,7,10,11,17), Sharangpani taught branch processing and prediction logic (e.g., see col. 6, lines 32-col. 7, line 31) where the instruction sequence predicted to be executed and the instruction sequence predicted not to be executed were determined and a determination if the predictions were correct and then restoration was done in parallel to the instruction pipeline stages (e.g., see col. 7, lines 32-59 and col. 3, line 41-col. 4, line 46, and col. 11, lines 25-59). Further as to claims 12, 13,14 in order to access a cache for restoring data a read signal would have been required. As to a mispredicted memory control unit sending the signal and a mispredicted data line Sharangpani taught branch processing control logic (e.g., see fig. 3) for processing branch instructions by fetching both paths that are both executed and the when the branch is resolved the correct path is restored (e.g., see col. 2, lines 26-42 and col. 7, lines 32-59 and col. 3, line 41-col. 4, line 30, and col. 11, lines 25-59). This would have required coupling the memory or cache to the pipelines and storing the correct data in to the cache and then storing the correct data to the

pipeline stages for restoring the correct instructions and data to the pipeline stages. Also since one reason for processing both paths simultaneously was to save time or cycles in the processing of the instructions then one of ordinary skill would have been motivated to incorporate path lines for transfer of data to/from both paths to/from memory or cache. For the mispredicted path this would have comprised a mispredicted data line and recovery branch data line to each couple each stage of the instruction pipeline stages to the mispredicted path side memory and to store/restore the result to/from the mispredicted path side.

Allowable Subject Matter

8. Claims 15,16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mowry (patent No. 5,696,958) disclosed a DP system for reducing delays following execution of a branch instruction in an instruction pipeline (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER